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Edition 1.0 2018-10

INTERNATIONAL STANDARD

Radio data system (RDS) – VHF/FM sound broadcasting in the frequency range from 64,0 MHz to 108,0 MHz – Part 1: Modulation characteristics and baseband coding

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RADIO DATA SYSTEM (RDS) – VHF/FM SOUND BROADCASTING IN THE FREQUENCY RANGE FROM 64,0 MHz TO 108,0 MHz –

Part 1: Modulation characteristics and baseband coding

FOREWORD

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International Standard IEC 62106-1 has been prepared by technical area 1: Terminals for audio, video and data services and contents, of IEC technical committee 100: Audio, video and multimedia systems and equipment.

This first edition, together with IEC 62106-2, IEC 62106-3, IEC 62106-4, IEC 62106-5 and IEC 62106-6, cancels and replaces IEC 62106:2015, and constitutes a technical revision.

This edition includes the following significant technical changes with respect to IEC 62106:2015:

- Provision has been made to carry RDS on multiple data-streams (RDS2).

The text of this International Standard is based on the following documents:

CDV	Report on voting
100/2907/CDV	100/3055/RVC

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 62106 series, published under the general title *Radio data system (RDS) – VHF/FM sound broadcasting in the frequency range from 64,0 MHz to 108,0 MHz*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

INTRODUCTION

Since the mid-1980s a fascinating development has taken place. Most of the multimedia applications and standards have been created or redefined significantly. Hardware has become extremely powerful with dedicated software and middleware. In the mid-1980s, Internet as well as its protocols did not exist. Navigation systems became affordable in the late 1990s, and a full range of attractive smartphones now exist. The computing power of all these new products is comparable with that of the mainframe installations in that era.

Listener expectations have grown faster than the technology. Visual experience is now very important, like the Internet look and feel. Scrolling text or delivering just audio is nowadays perceived as insufficient for FM radio, specifically for smartphone users. New types of radio receivers with added value features are therefore required. RDS has so far proven to be very successful.

FM radio with RDS is an analogue-digital hybrid system, which is still a valid data transmission technology and only the applications need adaptation. Now the time has come to solve the only disadvantage, the lack of sufficient data capacity. With RDS2, the need to increase the data capacity can be fulfilled.

RDS was introduced in the early 1980s. During the introductory phase in Europe, the car industry became very involved and that was the start of an extremely successful roll-out. Shortly afterwards, RDS (RBDS) was launched in the USA [1, 2, 3, 4, 5].[1]

The RDS Forum has investigated a solution to the issue of limited data capacity. For RDS2, both sidebands around the RDS 57 kHz subcarrier can be repeated a few times, up to three, centred on additional subcarriers higher up in the FM multiplex still remaining compatible with the ITU Recommendations.

The core elements of RDS2 are the additional subcarriers, which will enable a significant increase of RDS data capacity to be achieved, and then only new additional data applications will have to be created, using the RDS-ODA feature, which has been part of the RDS standard IEC 62106 for many years.

In order to update IEC 62106:2015 to the specifications of RDS2, IEC 62106 has been restructured as follows:

Part 1: Modulation characteristics and baseband coding

Part 2: RDS message format, coding and definition of RDS features

Part 3: Usage and registration of Open Data Applications ODAs

Part 4: Registered code tables

Part 5: Marking of RDS and RDS2 devices

Part 6: Compilation of technical specifications for Open Data Applications in the public domain

The following future parts are planned:

Part 7: RBDS

Part 8: Universal Encoder Communication Protocol UECP

The original specifications of the RDS system have been maintained and the extra functionalities of RDS2 have been added.

Obsolete or unused functions from the original RDS standard IEC 62106:2015 have been deleted. The presentation in Parts 1, 2 and 3 follows the OSI basic reference model for information processing systems [6].

_____

1 Numbers in square brackets refer to the Bibliography.

RADIO DATA SYSTEM (RDS) – VHF/FM SOUND BROADCASTING IN THE FREQUENCY RANGE FROM 64,0 MHz TO 108,0 MHz –

Part 1: Modulation characteristics and baseband coding

1 Scope

This part of IEC 62106 defines the basic layer of the Radio Data System (RDS) intended for application to VHF/FM sound broadcasts in the range 64,0 MHz to 108,0 MHz, which can carry either stereophonic (pilot-tone system) or monophonic programmes (as stated in ITU-R Recommendation BS.450-3 and ITU-R Recommendation BS.643-3).

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 62106 (all parts), *Radio Data System (RDS) – VHF/FM sound broadcasting in the frequency range from 64,0 MHz to 108,0 MHz*

ITU-R Recommendation BS.450-3, *Transmission standards for FM sound broadcasting at VHF*

ITU-R Recommendation BS.643-3, *Radio data system for automatic tuning and other applications in FM radio receivers for use with pilot-tone system*

3 Terms, definitions and abbreviated terms

3.1 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1.1
data-stream
data modulated on any RDS subcarrier

3.2 Abbreviated terms

AM Amplitude Modulation

FM Frequency Modulation

MF Medium wave broadcasting Frequency band

NOTE 1 MF applies to ITU, all Regions.

LF Long wave broadcasting Frequency band

NOTE 2 LF applies to ITU, Region 1 only.

VHF Very High Frequency broadcasting band

NOTE 3 VHF applies only to ITU.

RDS Radio Data System

NOTE 4 RDS is the generic term for Radio Data System. It designates also the legacy RDS system of all previous editions of IEC 62106, but it uses only the basic stream 0 on subcarrier 57 kHz.

RDS2 Radio Data System 2

NOTE 5 RDS2 is the generic term for Radio Data System 2. It designates Radio Data System comprising data-stream 0 on a 57 kHz subcarrier and one or more additional data-streams (1, 2, 3) on higher frequency subcarriers.

RBDS Radio Broadcast Data System

NOTE 6 RBDS is a variant of RDS, see [5].

3.3 Notation and conventions

3.3.1 Hexadecimal notation

C notation “0x” designates hex (base 16) numbers.

NOTE This notation is used throughout this standard.

3.3.2 Nomenclature for group types

Group types A and B are referenced by a number 0…15 and a version A or B. Group type C is referenced by a header byte and 7 data bytes

3.3.3 Capitalized RDS terms

To align with general usage, some technical terms are capitalized throughout the IEC 62106 series, such as "Radio Data System" and "Radio Broadcast Data System".

4 Modulation characteristics of the data channels

4.1 General

The Radio Data System is intended for application to VHF/FM sound broadcasting transmitters in the range from 64,0 MHz to 108,0 MHz, which carry stereophonic (pilot-tone system) or monophonic sound broadcasts specified in ITU-R Recommendation BS.450-3.

The data-streams are carried on up to four subcarriers, which are added to the stereo multiplex signal (or monophonic signal, as appropriate) at the input of the VHF/FM transmitter. Block diagrams of the data source equipment at the transmitter and a typical receiver arrangement are shown for RDS in Figure 1 and Figure 2, respectively.

4.2 Subcarrier generation

During stereo broadcasts, the subcarrier frequencies are derived from and phase-locked to the 19 kHz pilot-tone. The tolerance of the subcarriers is directly related to the tolerance of the 19 kHz pilot-tone, which is ± 2 Hz (ITU-R Recommendation BS.450-3).

During monophonic broadcasts, the frequency of the data-stream 0 subcarrier is 57 kHz ± 6 Hz. RDS2 data-stream 1, 2 and 3 subcarriers are locked to the data-stream 0 subcarrier.

Data-stream 0 subcarrier is required for RDS and RDS2 while data-stream 1, 2 and 3 subcarriers are optional and are only applicable to RDS2.

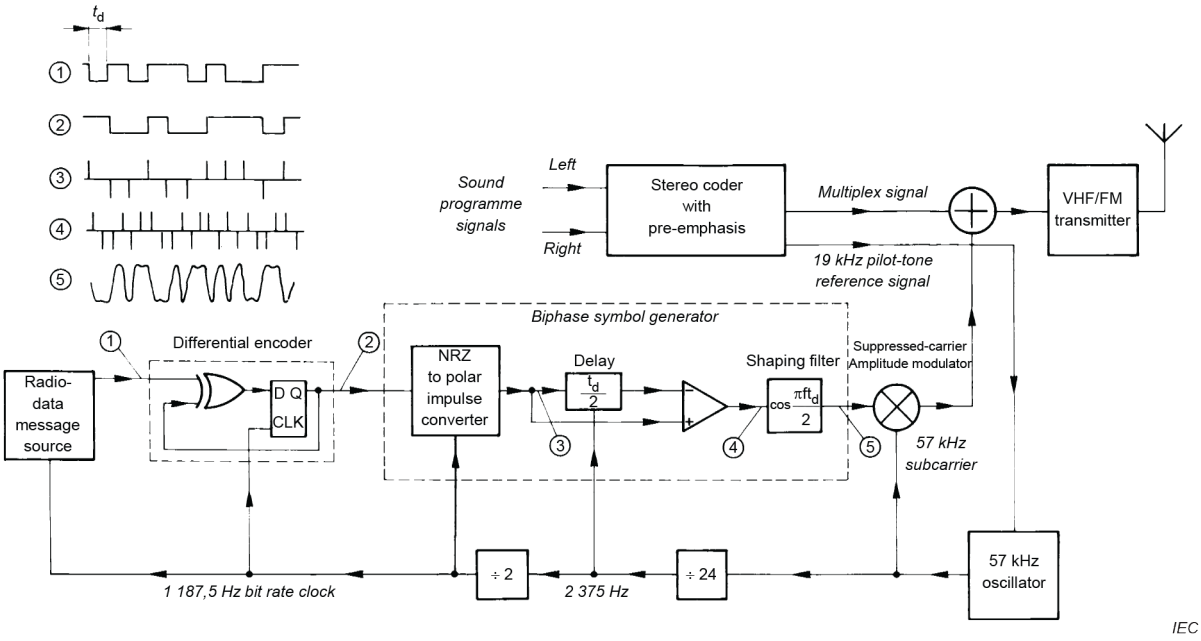
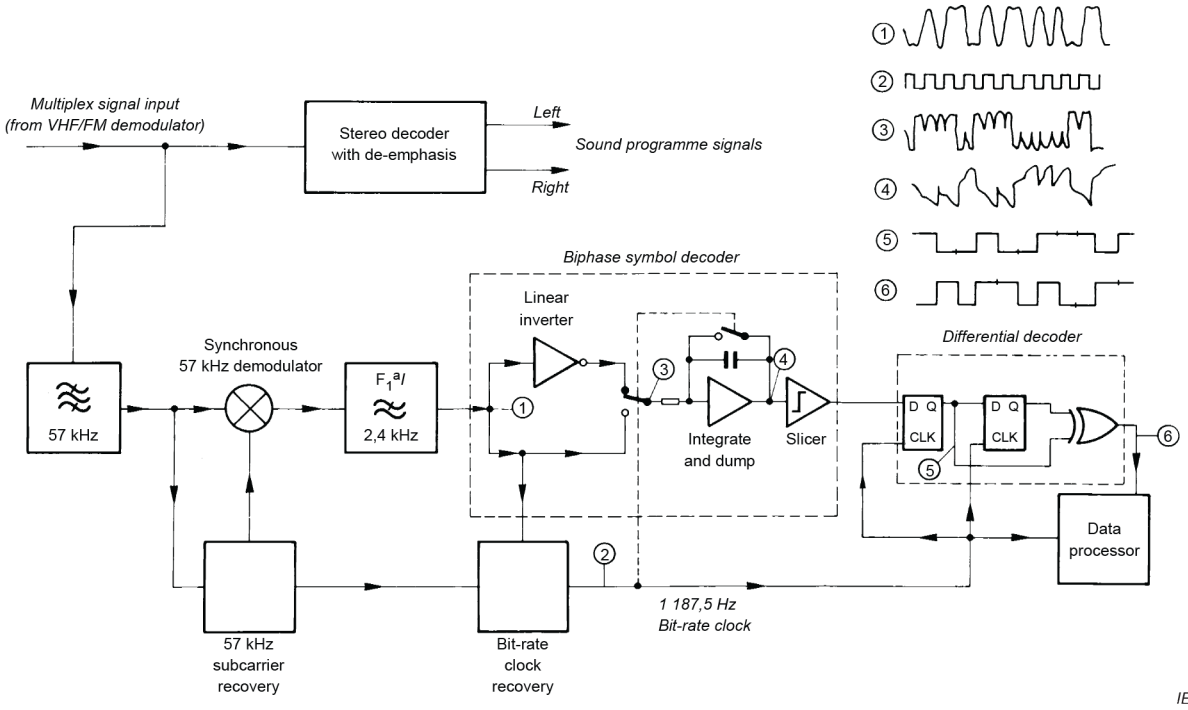


Figure 1 – Block diagram of data-stream 0 radio-data equipment at the transmitter



[a] The overall data-shaping in this decoder comprises the filter F1 and the data-shaping inherent in the biphase symbol decoder. The amplitude/frequency characteristic of filter F1 is therefore not the same as that given in Figure 4.

Figure 2 – Block diagram of a typical data-stream 0 radio-data receiver/decoder

4.3 Data-stream subcarrier frequencies for all possible streams

The data-stream subcarriers are as in Figure 3.

Data-stream 0: 57,0 kHz (3 × pilot-tone)

Data-stream 1: 66,5 kHz

Data-stream 2: 71,25 kHz

Data-stream 3: 76,0 kHz (4 × pilot-tone)

The theoretically possible 61,75 kHz data-stream subcarrier is not used.

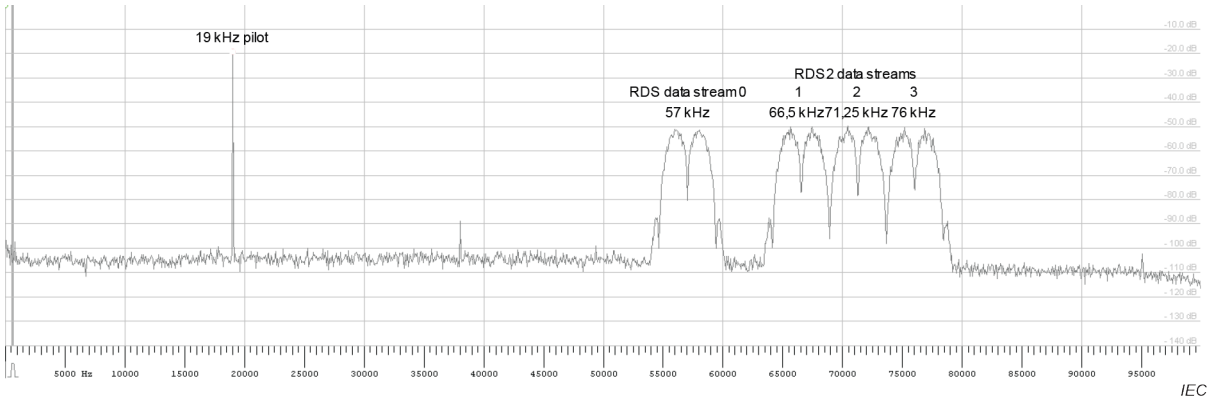


Figure 3 – Subcarriers for RDS data-stream 0 and additional RDS2 data-streams 1, 2 and 3

4.4 Subcarrier phase requirements

During stereo broadcasts, the subcarrier for data-stream 0 shall be locked either in phase or in quadrature to the 19 kHz pilot-tone. The tolerance on this phase angle is ± 10°, measured at the modulation input to the FM transmitter. The subcarriers for data-streams 1, 2 and 3 shall be locked in phase to the subcarrier for data-stream 0, so that all subcarriers periodically have 0 phase at the same time, nominally repeating every 4/19 ms.

4.5 Subcarrier level requirements

The maximum permitted deviation due to the composite multiplex signal is ± 75 kHz. In order to support additional subcarriers, the deviation will have to be reduced on other elements in the multiplex MPX spectrum to keep within the maximum deviation requirement.

The minimum recommended deviation for data-stream 0 subcarrier is 1,5 kHz. Optimal performance is achieved at 2 kHz of deviation for data-stream 0.

The number of subcarriers utilized and their relative levels may be adjusted in order to meet the desired output deviation and subcarrier coverage area.

The ITU has recommendations for the amount of deviation to use for elements of the MPX spectrum. The overall transmission shall meet the ITU requirements.

NOTE With the 2 kHz injection level of the subcarrier, the level of each sideband of the subcarrier corresponds to half the nominal peak deviation level of 2 kHz for an all-zeroes message data-stream (i.e. a continuous bit-rate sine-wave after biphase encoding).

4.6 Data-stream modulation requirements

Each subcarrier is amplitude-modulated by the shaped and biphase coded data signal (see 4.9). The subcarrier itself is suppressed. This method of modulation may alternatively be thought of as a form of two-phase phase-shift-keying (PSK) with a phase deviation of ±90°.

4.7 Clock-frequency and data-rate

The clock-frequency for data-stream 0 subcarrier 57 kHz is obtained by dividing the transmitted subcarrier frequency by 48. Consequently, the basic data-rate for data-stream 0 (see Figure 1) is 1 187,5 bit/s ± 0,125 bit/s.

The frequencies for the data-stream 1-3 subcarriers can be calculated by addition of the ¼ pilot frequencies: 19/4 = 4,75 kHz. The first position, 61,75 kHz is not used to protect the basic subcarrier of 57 kHz on existing receivers.

This results in subcarrier frequencies as shown in 4.3 and Figure 3. The data rate for data-streams 1, 2 and 3 are the same as for data-stream 0.

4.8 Differential coding on all data-streams

The source data at the transmitter are differentially encoded according to the following rules, see Table 1.

Table 1 – Encoding rules

Previous output (at time t_{i-1})	New input (at time t_i)	New output (at time t_i)
0	0	0
0	1	1
1	0	1
1	1	0
t_i is some arbitrary time and t_{i-1} is the time one message-data clock-period earlier, and where the message-data clock-rate is equal to 1 187,5 Hz.		

Thus, when the input-data level is 0, the output remains unchanged from the previous output bit, and when an input 1 occurs, the new output bit is the complement of the previous output bit.

In the receiver, the data may be decoded by the inverse process, see Table 2.

Table 2 – Decoding rules

Previous input (at time t_{i-1})	New input (at time t_i)	New output (at time t_i)
0	0	0
0	1	1
1	0	1
1	1	0

The data is thus correctly decoded whether or not the demodulated data signal is inverted.

4.9 Data-channel spectrum shaping on all data-streams

The power of the data signal at and close to each data-stream subcarrier is minimized by coding each source data bit as a biphase symbol.

This is done to avoid data-modulated cross-talk in phase-locked-loop stereo decoders. The principle of the process of generation of the shaped biphase symbols is shown schematically in Figure 1. In concept, each source bit gives rise to an odd impulse-pair, e(t), so that a logic 1 at source gives:

$$e(t) = \delta(t) - \delta(t + t_d / 2) \quad (1)$$

and a logic 0 at source gives:

$$e(t) = -\delta(t) + \delta(t + t_d / 2) \quad (2)$$

These impulse-pairs are then shaped by a filter $H_T(f)$, to give the required band-limited spectrum where

$$H_T(f) = \begin{cases} \cos\dfrac{\pi f t_d}{4} & \text{if } 0 \le f \le 2/t_d \\ 0 & \text{if } f > 2/t_d \end{cases} \quad (3)$$

and where

$$t_d = \frac{1}{1\,187{,}5}\text{s}$$

The data-spectrum shaping filtering has been split equally between the transmitter and receiver (to give optimum performance in the presence of random noise) so that, ideally, the data filtering at the receiver should be identical to that of the transmitter, i.e. as given above in Equation (3). The overall data-channel spectrum shaping $H_O(f)$ would then be 100 % cosine roll-off.

The specified transmitter and receiver low-pass filter responses, as defined in Equation (3), are illustrated in Figure 4, and the overall data-channel spectrum shaping is shown in Figure 5.

The spectrum of the transmitted biphase-coded radio-data signal is shown in Figure 6 and the time-function of a single biphase symbol (as transmitted) in Figure 7.

For example, the 57 kHz modulated data signal at the output of the source equipment can be seen in the photograph of Figure 8.

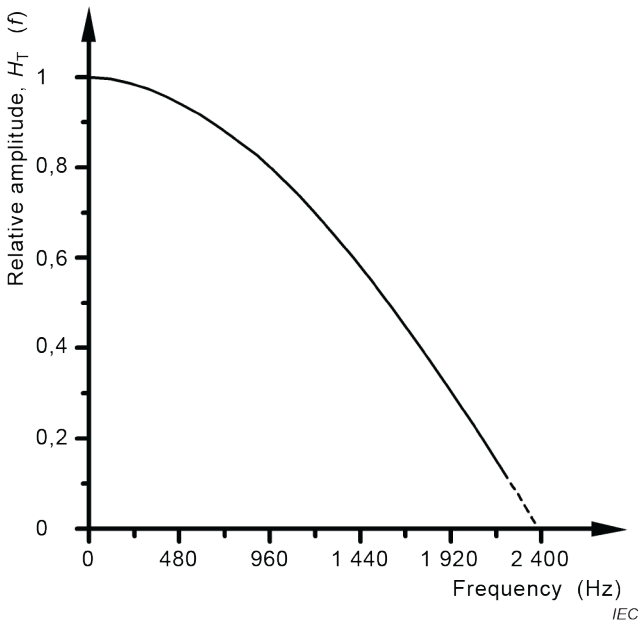


Figure 4 – Amplitude response of the specified transmitter or receiver data-shaping filter

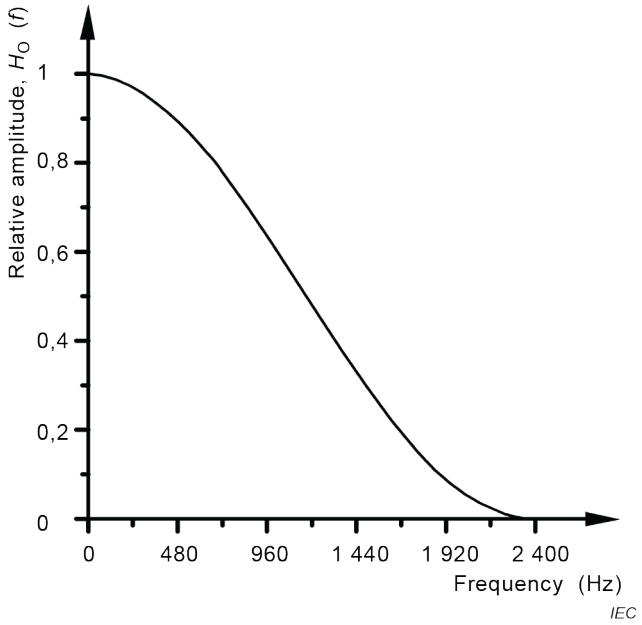


Figure 5 – Amplitude response of the combined transmitter and receiver data-shaping filters

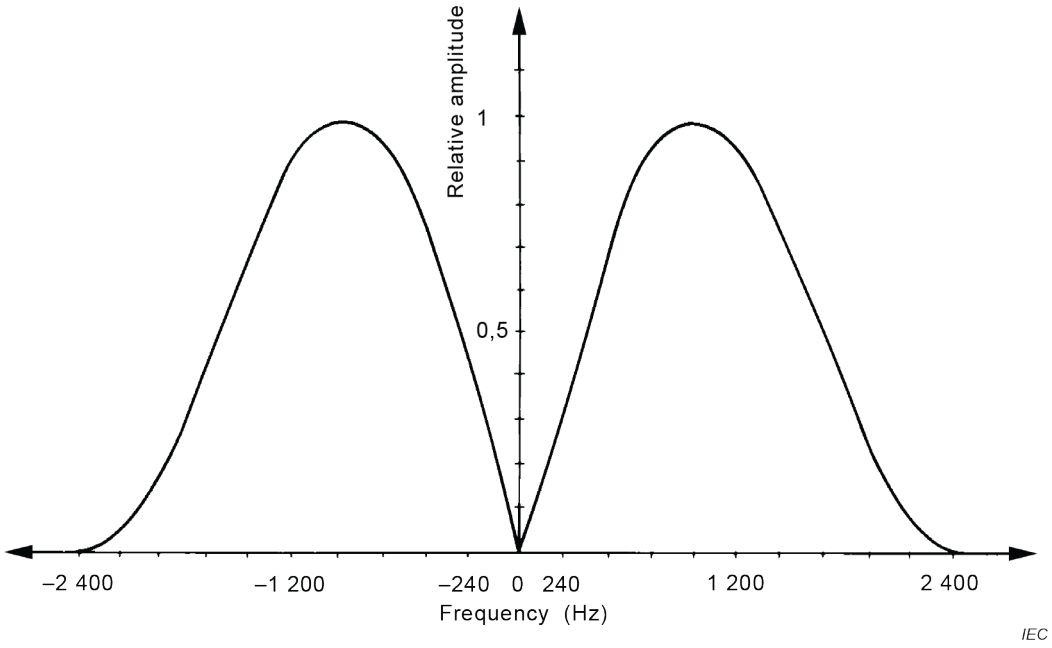


Figure 6 – Spectrum of biphase coded radio-data signals

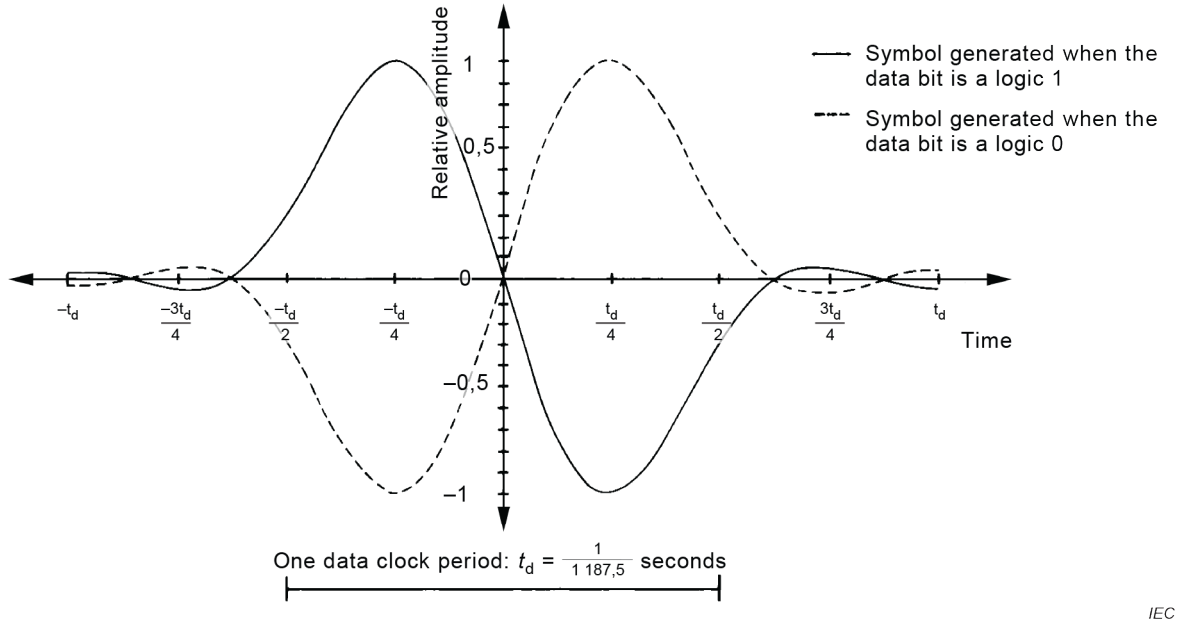


Figure 7 – Time-function of a single biphase symbol

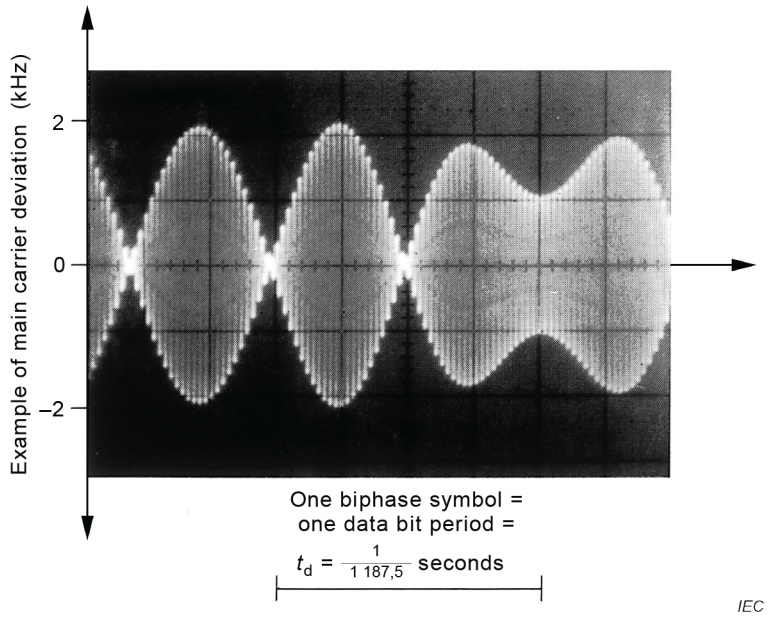


Figure 8 – 57 kHz modulated data-signal

4.10 Symbol phase shifts of data across data-streams

The additional RDS2 data-streams increase the FM peak-deviation. The total RDS2 peak-deviation when transmitting all four data-streams (with in-phase symbols) would be increased by a factor of 4.

By making use of a phase shift of a quarter-symbol between the data-streams, the total peak-deviation will only increase by a factor of 3.

Regardless of the number of data-streams in use, the phase shifts shown in Table 3 with respect to data-stream 0 shall be applied to accommodate for optimal peak-deviation.

Table 3 – Phase shifts of data across data-streams 1-3 with respect to data-stream 0

RDS data-stream	RDS subcarrier	Symbol phase shift
0	57 kHz	0
1	66,5 kHz	½
2	71,25 kHz	¼
3	76 kHz	¾

5 Baseband coding

5.1 Data-stream baseband coding structure

Figure 9 shows the structure of the baseband coding. The largest element in the structure is called a group of 104 bits each. Each group comprises 4 blocks of 26 bits each. Each block comprises an information word and a checkword. Each information word comprises 16 bits. Each checkword comprises 10 bits (see 5.2).

All information words, checkwords, binary numbers or binary address values have their most significant bit (MSB) transmitted first (see Figure 9). Thus, the last bit transmitted in a binary number or address has weight 2^0.

The data transmission is fully synchronous and there are no gaps between the groups or blocks.

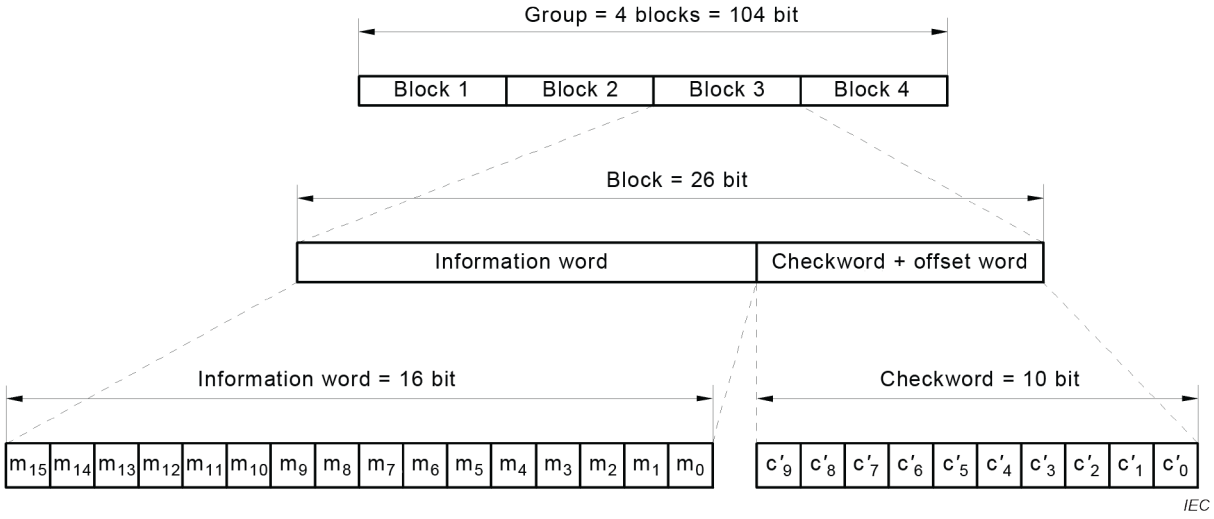


Figure 9 – Structure of the baseband coding

5.2 Data-stream error protection

Each transmitted 26-bit block contains a 10-bit checkword which is primarily intended to enable the receiver/decoder to detect and correct errors which occur in transmission. This checkword (i.e. c'_9, c'_8, ... c'_0 in Figure 9) is the sum (modulo-two) of

a) the remainder after multiplication by *x10* and then division (modulo-two) by the generator polynomial $g(x)$, of the 16-bit information word;

b) a 10-bit binary string $d(x)$, called the offset word;

where the generator polynomial, $g(x)$ is given by

$$g(x) = x^{10} + x^8 + x^7 + x^5 + x^4 + x^3 + 1$$

and where the offset values, $d(x)$, which are different for each block within a group (see 5.3), are given in Annex A.

The purpose of adding the offset word is to provide a group and block synchronization system in the receiver/decoder (see 5.3). Because the addition of the offset is reversible in the decoder, the normal additive error-correcting and detecting properties of the basic code are unaffected.

The checkword thus generated is transmitted with its most significant bit (i.e. the coefficient of c'_9 in the checkword) first and is transmitted at the end of the block which it protects.

The above description of the error protection may be regarded as definitive, but further explanatory notes on the generation and theory of the code are given in Annex B and Annex C.

The error-protecting code has the following error-checking capabilities [7, 8]:

1) detects all single and double bit errors in a block;
2) detects any single error burst spanning 10 bits or less;
3) detects about 99,8 % of bursts spanning 11 bits and about 99,9 % of all longer bursts.

The code is also an optimal burst error correcting code [9] and is capable of correcting any single burst of span 5 bits or less.

5.3 Synchronization of blocks and groups across all streams

The blocks within each group are identified by the offset words A, B, C or C', and D added to blocks 1, 2, 3, and 4, respectively, in each group (see Annex A).

The beginnings and ends of the data blocks may be recognized in the receiver decoder by using the fact that the error-checking decoder will, with a high level of confidence, detect any block synchronization slip as well as additive errors. This system of block synchronization is made reliable by the addition of the offset words (which also serve to identify the blocks within the group). These offset words destroy the cyclic property of the basic code so that in the modified code, cyclic shifts of codewords do not give rise to other codewords [10, 11].

Further explanation of a technique for extracting the block synchronization information at the receiver is given in Annex C.

Blocks in data-streams 1, 2 and 3 shall align with the same blocks in data-stream 0. For example, each block 1 in data-streams 1, 2 and 3 is transmitted synchronously with block 1 in data-stream 0. This allows for efficient decoding of multiple streams in receivers.

6 Transmission options on data-streams 1, 2 and 3

The transmission operator has the flexibility to decide how many (one, two or three) of the data-streams 1, 2 and 3 they wish to transmit. Changes to which data-streams are transmitted should be avoided (or at least limited in the long-term) in order to avoid disturbances to the received audio signal. Furthermore, there is the flexibility to decide the mix of data transmitted across the chosen data-streams 1, 2 and 3. Depending on the nature of the application, consideration should be made of the following factors.

a) Load balancing – It may be advantageous to spread data across multiple data-streams in parallel to help balance the load and increase data throughput.

b) Reliability – Statistically there is a slight difference in data transmission reliability between the data-streams, reliability degrading as the subcarrier frequency increases. This means that data-stream 1 is slightly more reliable than data-stream 2 and likewise data-stream 2 slightly more reliable than data-stream 3. This may factor into decisions of data placement and data repetition rates on each data-stream.

Annex A
(normative)

Offset words to be used for group and block synchronization

The offset words are chosen in such a way that the content in the offset register will not be interpreted as a burst of errors equal to or shorter than five bits when rotated in the polynomial shift register (see Annex B).

Only eight bits (i.e. d_9 to d_2) are used for identifying the offset words. The remaining two bits (i.e. d_1 and d_0) are set to logical level zero.

The five offset words (A, B, C, C', D) of Table A.1 are used for all applications.

Table A.1 – Offset word codes

Offset word[a]	Binary value									
	d_9	d_8	d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0
A	0	0	1	1	1	1	1	1	0	0
B	0	1	1	0	0	1	1	0	0	0
C	0	1	0	1	1	0	1	0	0	0
C'	1	1	0	1	0	1	0	0	0	0
D	0	1	1	0	1	1	0	1	0	0

[a] In previous editions of IEC 62106 the offset word E (binary value = 0) was used in the USA when RDS and MMBS (Modified Mobile Search paging) were implemented. This service has been discontinued and therefore there is no longer a need for new receivers to interpret offset word E.

The offset words are added (modulo-two) to the checkword c_9 to c_0 to generate the modified check-bits: $c'_9 – c'_0$ (see 5.2).

Annex B
(informative)

Theory and implementation of the modified shortened cyclic code

B.1 General

The data format described in this document uses a shortened cyclic block code, which is given the capability of detecting block-synchronization-slip by the addition (modulo-two) of chosen binary sequences (offset words, see Annex A) to the check bits of each codeword, see references [8, 10 and 11].

B.2 Encoding procedure

B.2.1 Theory

A definitive description of decoding of information is given in B.3.2.

The code used is an optimum burst-error-correcting shortened cyclic code and has the generator polynomial:

$$g(x) = x^{10} + x^8 + x^7 + x^5 + x^4 + x^3 + 1$$

Each block consists of 16 information bits and 10 check bits. Thus, the block length is 26 bits.

The 10-bit checkword of the basic shortened cyclic code may be formed in the usual way, i.e. it is the remainder after multiplication by x^{n-k} (where $n-k$ is the number of check bits, 10 here), and then division (modulo-two) by the generator polynomial $g(x)$, of the message vector.

Thus, if the polynomial

$$m(x) = m_{15}x^{15} + m_{14}x^{14} + \ldots + m_1 x + m_0$$

(where the coefficients m_n are 0 or 1) represents the 16-bit message vector, the basic code vector $v(x)$ is given by

$$v(x) = m(x)x^{10} + \left| \frac{m(x)x^{10}}{g(x)} \right| \bmod g(x)$$

The transmitted code vector is then formed by the addition (modulo-two) of the 10-bit offset word, $d(x)$ (see Annex A) to the basic code vector $v(x)$.

Thus, the transmitted code vector, $c(x)$, is given by

$$c(x) = d(x) + v(x)$$

$$= d(x) + \left| \frac{m(x)x^{10}}{g(x)} \right| \bmod g(x)$$

The code vector is transmitted most significant bit first, i.e. information bits $c_{25}x^{25}$ to $c_{10}x^{10}$, followed by modified check bits c'_9x^9 to c'_0x^0.

The encoding process may alternatively be considered in terms of its generator matrix $\mathbf{G}$, shown in Figure B.1, which is derived from the generator polynomial. The 16 information bits are expressed as a 16 × 1 column matrix and multiplied by the generator matrix to give the information bits and check bits. The complete transmitted code vector is then formed by the addition of the offset word, $d(x)$.

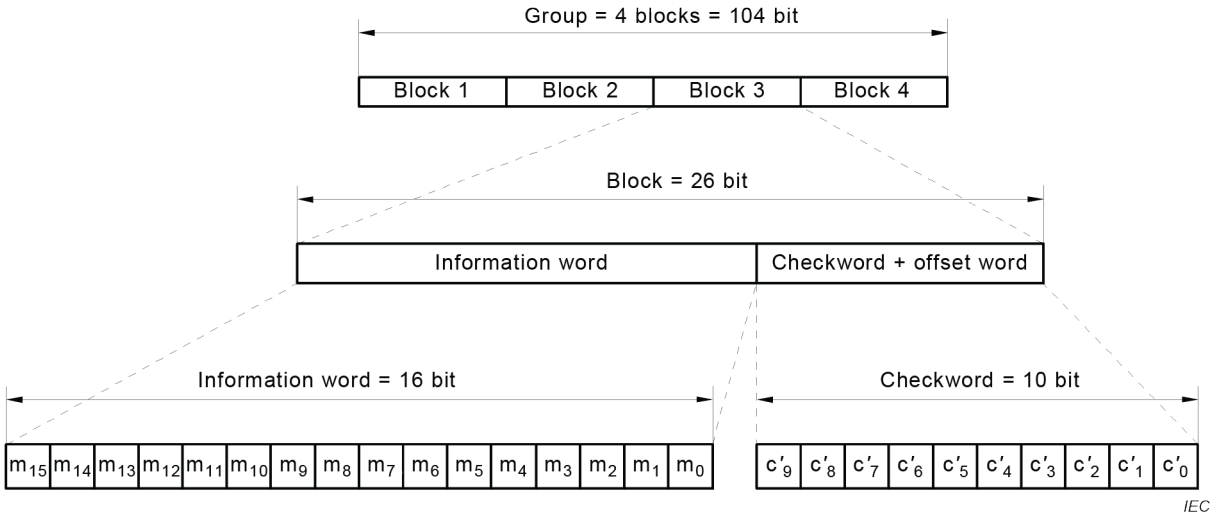


Figure B.1 – Generator matrix of the basic shortened cyclic code in binary notation

Thus

$$(m_{15}x^{15} + m_{14}x^{14} + \ldots + m_0)\ \mathbf{G} = m_{15}x^{25} + m_{14}x^{24} + \ldots + m_0x^{10} + c_9x^9 + c_8x^8 + \ldots + c_0x^0$$

where

$$c_9 = (m_{15} \times 0) \oplus (m_{14} \times 1) \oplus (m_{13} \times 1) \oplus \ldots \oplus (m_1 \times 1) \oplus (m_0 \times 0)$$

$$c_8 = (m_{15} \times 0) \oplus (m_{14} \times 0) \oplus (m_{13} \times 1) \oplus \ldots \oplus (m_1 \times 1) \oplus (m_0 \times 0), \text{ etc.}$$

($\oplus$ indicates modulo-two addition).

The check bits of the code vector are thus readily calculated by the modulo-two addition of all the rows of the generator matrix for which the corresponding coefficient in the message vector is "1".

Thus for the message vector:

$$m(x) = 0000000000000001$$

The corresponding code vector is:

$$v(x) = 0000000000000010110111001$$

which is the bottom row of the generator matrix.

After adding the offset word, say $d(x)$ = 0110011000, the transmitted code vector is:

$$c(x) = 0000000000000010000100001$$

Similarly for the all "1"s message vector:

$$m(x) = 1111111111111111$$

it follows that:

$$v(x) = 1111111111111110011001101$$

which on adding an offset word $d(x)$ = 0110011000 becomes:

$$c(x) = 1111111111111110101010101$$

B.2.2 Shift-register implementation of the encoder

Figure B.2 shows a shift-register arrangement for encoding the transmitted 26-bit blocks. The encoding procedure is as follows:

a) At the beginning of each block, the 10-bit encoder shift-register is cleared to the "all-zeroes" state.

b) With Gates A and B open (i.e. data passes through) and Gate C closed (data does not pass through), the 16-bit message string is clocked serially into the encoder and simultaneously out to the data channel.

c) After all the 16 information bits for a block have been entered, Gates A and B are closed and Gate C opened.

d) The encoder shift-register is then clocked a further 10 times to shift the checkword out to the data channel through a modulo-two adder where the offset word, $d(x)$, appropriate to the block is added serially bit-by-bit to form the transmitted checkword.

e) The cycle then repeats with the next block.

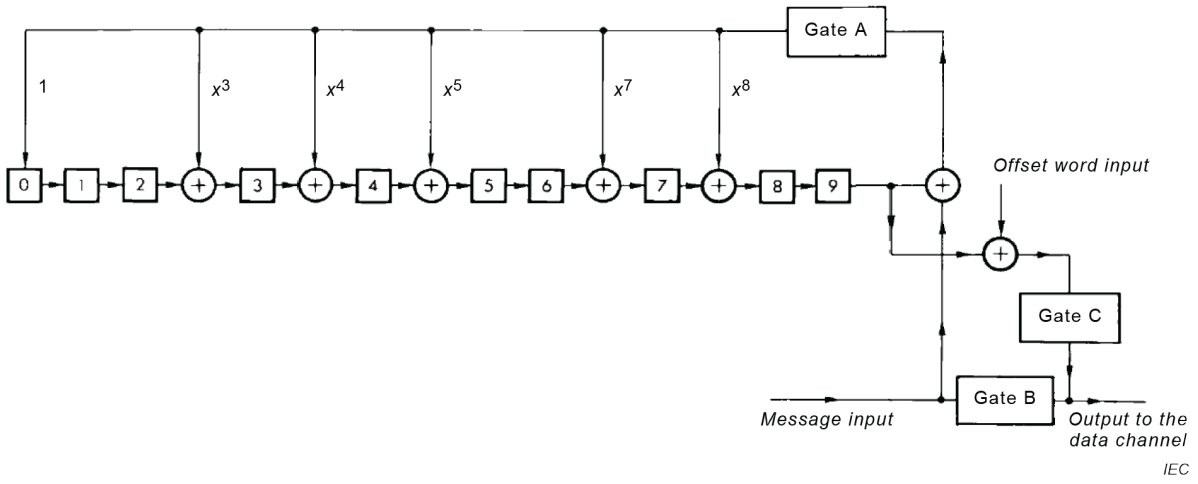


Figure B.2 – Shift-register implementation of the encoder

B.3 Decoding procedure

B.3.1 Theory

For a received binary sequence, $\bar{y}$, the syndrome $\bar{s}$ can be calculated as $\bar{s} = \bar{y}\mathbf{H}$, where $\mathbf{H}$ is a parity-check matrix such as that given in Figure B.3. If $\bar{x}$ is the transmitted binary sequence and $\bar{y}$ is the received sequence, then $\bar{y} \oplus \bar{x}$ is a sequence that contains a 1 in each position in which $\bar{x}$ and $\bar{y}$ differ. This sequence is called the error sequence $\bar{z}$. The definition of the parity-check matrix $\mathbf{H}$ is such that $\bar{x}\mathbf{H} = 0$ $\bar{x}\mathrm{H} = 0$, if $\bar{x}$ is a codeword.

Thus $$\bar{z}\mathbf{H} = (\bar{y} \oplus \bar{x}) = \bar{y}\mathbf{H} \oplus \underbrace{\bar{x}\mathbf{H}}_{=0} = \bar{y}\mathbf{H} = \bar{s}$$

i.e. $$\bar{s} = \bar{z}\mathbf{H}$$

If the errors introduced on the channel are known then the syndrome is also known. This relation is used for synchronization in the system.

If an offset word is added to each block, it is the same as an error added to each block, i.e. the offset word is equivalent to an error sequence $\bar{z}$, on the channel. If there are no other errors on the channel, the offset word can be found in the received information by calculating the syndrome $\bar{s} = \bar{z}\mathbf{H}$.

The calculation of the syndromes for the different offset words can easily be done by multiplying each word with the parity matrix $\mathbf{H}$.

For example, with the offset word A = 0011111100:

$$\bar{z} = \underset{\uparrow m_{15}}{0000000000000000} \;\Big|\; \underset{m_0 \uparrow}{0011111100} \Big|$$
$$\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad \uparrow c_9 \quad c_0 \uparrow$$

Now the parity-check matrix $\mathbf{H}$ is:

$$\mathbf{H} = \begin{vmatrix} 1000000000 \\ 0100000000 \\ 0010000000 \\ 0001000000 \\ 0000100000 \\ 0000010000 \\ 0000001000 \\ 0000000100 \\ 0000000010 \\ 0000000001 \\ 1011011100 \\ 0101101110 \\ 0010110111 \\ 1010000111 \\ 1110011111 \\ 1100010011 \\ 1101010101 \\ 1101110110 \\ 0110111011 \\ 1000000001 \\ 1111011100 \\ 0111101110 \\ 0011110111 \\ 1010100111 \\ 1110001111 \\ 1100011011 \end{vmatrix}$$

IEC

This is the matrix which is used in the decoder of Figure B.4.

Figure B.3 – Parity-check matrix of the basic shortened cyclic code

Thus $\bar{s} = \bar{z}\mathbf{H}$ = 1111011000.

The other syndromes can be calculated in the same way. The syndromes corresponding to offset words A to D calculated using the matrix of Figure B.3, are shown in Table B.1.

Table B.1 – Offset word syndromes using matrix of Figure B.3

Offset	Offset word $d_9, d_8, d_7, \ldots d_0$	Syndrome $s_9, s_8, s_7, \ldots s_0$
A	0011111100	1111011000
B	0110011000	1111010100
C	0101101000	1001011100
C'	1101010000	1111001100
D	0110110100	1001011000

B.3.2 Implementation of the decoder

There are several methods using either hardware or software techniques for implementing the decoder. One possible method is described below.

Figure B.4 shows a shift-register arrangement for decoding the transmitted 26-bit blocks and performing error-correction and detection.

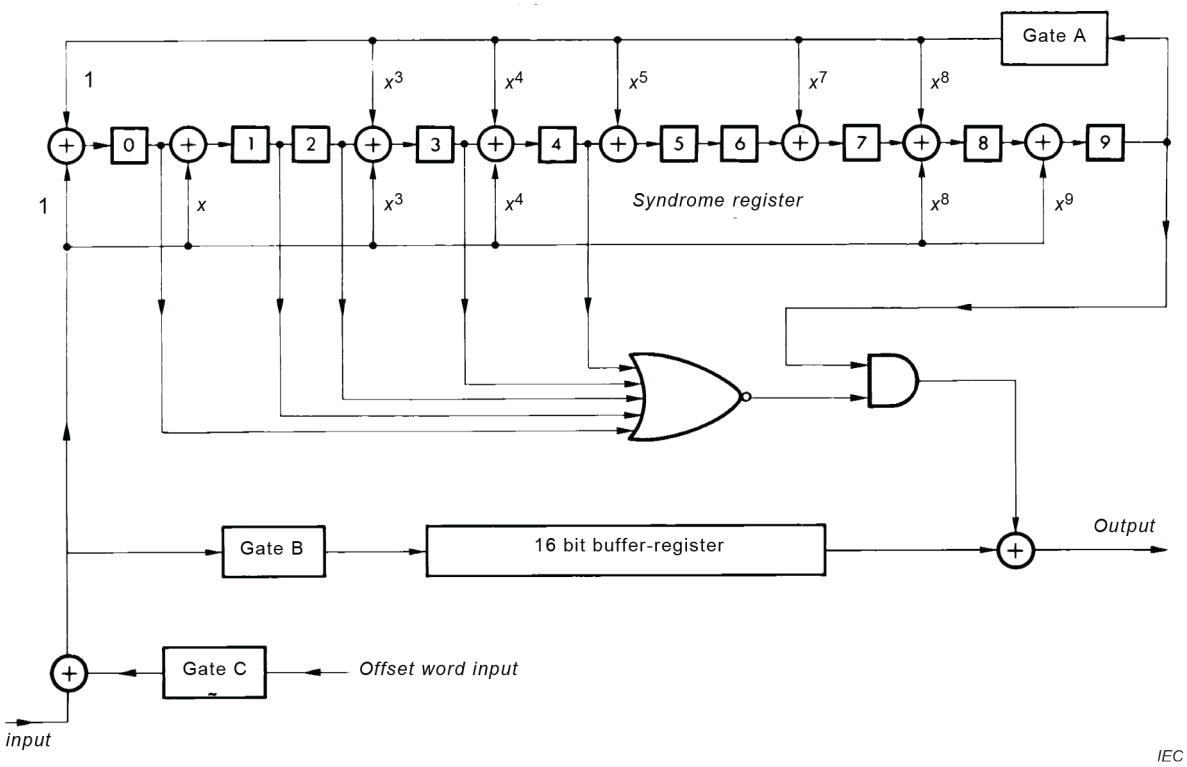


Figure B.4 – Shift-register implementation of the decoder

The decoding procedure is as follows, assuming that in this explanation, group and block synchronization have already been acquired (see Annex C).

a) At the beginning of each block the 10-bit syndrome-register and the 16-bit buffer-register are cleared to the "all-zeroes" state.

b) The 16 information bits are fed into the syndrome- and buffer-registers. Gates A and B are open (conducting), and Gate C is closed (not conducting).

c) With Gate B closed and Gate C open the 10 check-bits are fed into the syndrome-register. The offset word appropriate to the block is then subtracted from the checkword serially bit-by-bit at the modulo-two adder at the input to the decoder.

d) The 16 information bits in the buffer-register are clocked to the output and the content of the syndrome-register is rotated with Gate A open.

e) When the five left-most stages in the syndrome-register are all zero, a possible error burst with a maximum length of five bits shall lie in the five right-hand stages of the register.

f) Gate A is closed and the contents of the syndrome register are added bit-by-bit to the bit-stream coming from the buffer-register. If the five left-most stages do not become all zero before the buffer-register is empty, either an uncorrectable error has occurred or the error is in the check-bits;

g) The cycle then repeats with the next block.

In this implementation of the decoder, in addition to the connections to the syndrome register corresponding to the coefficients of the generator polynomial, $g(x)$, there is a second set of connections to perform automatic pre-multiplication of the received message by x^{325} modulo $g(x)$. This is necessary because the code has been shortened from its natural cyclic length of 341 bit. The remainder of x^{325} modulo $g(x)$ is: $x^9 + x^8 + x^4 + x^3 + x + 1$, and the second set of connections to the syndrome register corresponds to the coefficients in this remainder.

Reference [9] gives a further explanation of this decoding technique.

Annex C
(informative)

Implementation of group and block synchronization using the modified shortened cyclic code

C.1 Theory

C.1.1 Acquisition of group and block synchronization

To acquire group and block synchronization at the receiver (for example when the receiver is first switched on, on tuning to a new station, or after a prolonged signal-fade) the syndrome $\bar{s}$ shall be calculated for each received 26-bit sequence. That is, on every data-clock pulse the syndrome of the currently stored 26-bit sequence (with the most recently received data bit at one end and the bit received 26 clock pulses ago at the other) is calculated on every clock pulse.

This bit-by-bit check is done continuously until two syndromes corresponding to valid offset words, and in a valid sequence for a group, i.e. A, B, C (or C'), D are found $n \times 26$ bits apart (where n = 1, 2, 3, etc.). When this is achieved, the decoder is synchronized and the offset words which are added to the parity bits at the transmitter are subtracted at the receiver before the syndrome calculation for error correction/detection is done (see Annex B).

C.1.2 Detection of loss of synchronization

It is very important to detect loss of synchronization as soon as possible. One possibility is to check the syndrome continuously as for acquisition of synchronization. However, errors in the channel will make it difficult to continuously receive the expected syndromes, and therefore the decision shall be based on the information from several blocks, for example up to 50 blocks. Another possibility is to check the number of errors in each block and base the decision on the number of errors in 50 blocks.

One possibility for detecting block synchronization slips of one bit is to use the programme identification (PI) code, see IEC 62106-2 [12]. This does not usually change on any given transmission. If the known PI code is received correctly, but is found to be shifted one bit to the right or to the left, then a one bit clock-slip is detected. The decoder can then immediately correct the clock-slip.

C.2 Shift register arrangement for deriving group and block synchronization information

There are several methods using either hardware or software techniques for deriving group and block synchronization information. One possible method is described below. Figure C.1 shows a block diagram of a shift-register arrangement for deriving group and block synchronization information from the received data-stream. It comprises five main elements:

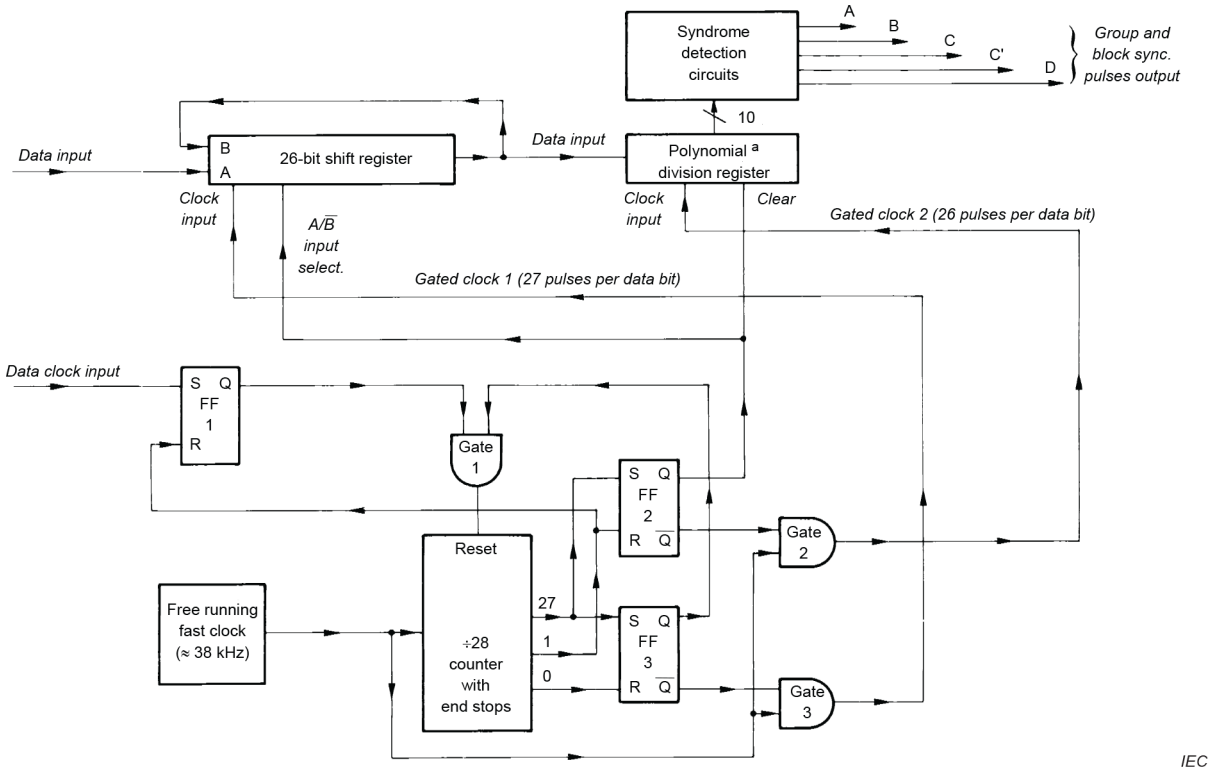
a) a 26-bit shift-register which may act either as a straight 26-bit delay (A/B input selector high) or as a recirculating shift-register (A/B input selector low);

b) a polynomial division circuit comprising a 10-bit shift-register with feedback taps appropriate to the generator polynomial, $g(x)$, described in 5.2 and Annex B;

c) a combinational logic circuit with five outputs indicating the presence of the "correct" syndromes resulting from the five offset words A, B, C, C' and D;

d) a fast-running clock operating with a frequency of at least 33,5 kHz;

e) a modulo-28 counter with endstops, decoding for states 0, 1 and 27, and associated logic gates 1 to 3 and flip-flops 1 to 3 (FF1 to FF3).



[a] The circuit of this register is represented in Figure B.2.

Figure C.1 – Group and block synchronization detection circuit

Assume that the modulo-28 counter is initially on its top endstop (state 27). Then FF2 and FF3 are set and FF1 is reset. The gated clocks to the 26-bit shift-register and the polynomial division circuit (gated clocks 1 and 2) are inhibited and the division circuit shift-register is cleared.

On the next data clock pulse FF1 is set, which in turn resets the modulo-28 counter to state 0. This resets FF3 which enables the fast clock (gated clock 1) to the 26-bit shift-register. This has its input A selected and thus the new data bit is entered into its left-hand end. The shift-register of the polynomial division circuit remains cleared and not clocked. On the next fast clock-pulse FF1 is reset ready for the next data clock-pulse.

Before then, however, the fast clock circulates the 26 bits at that time stored in the shift-register around, and thus passes them serially into the polynomial division shift-register where the syndrome (i.e. the remainder of the polynomial division) is calculated. If these 26 bits happened to be a valid code-word then the syndrome would be $x^{10}d(x)$ modulo $g(x)$. For example if the offset word is $d(x)$ = 0011111100, then the corresponding "correct" syndrome for that block would be 0101111111.

It should be noted that the syndromes obtained with this polynomial division register are different from that resulting from the matrix of Figure B.3 or the circuit of Figure B.4. The syndromes corresponding to offset words A to D are shown in Table C.1.

Table C.1 – Offset word syndromes for group and block synchronization

Offset	Offset word $d_9, d_8, d_7, \ldots d_0$	Syndrome $s_9, s_8, s_7, \ldots s_0$
A	0011111100	0101111111
B	0110011000	0000001110
C	0101101000	0100101111
C'	1101010000	1011101100
D	0110110100	1010010111

When the syndrome corresponding to one of the five offset words is found, a block synchronization pulse is given out of the appropriate one of the five outputs of the combinational logic circuit. With high probability (99,5 %) this will only occur when the stored 26 bits are a complete error-free block.

This decoding process shall all be achieved in less than one data-bit period ($\approx$ 842 µs).

On the next data-clock pulse the whole process repeats with the new data bit in the leftmost cell of the 26-bit shift-register and all the other bits shifted along one place to the right. Thus, a block synchronization pulse will usually be derived once every 26 bits and will mark the end of each received block.

Moreover, since the circuit identifies which offset word A, B, C, C' or D was added to the block, group synchronization is also achieved.

These group and block synchronization pulses cannot be used directly because with this system false synchronization pulses due to data mimicking or errors will occur. On average, (with random data) false synchronization pulses occur once in every 2×2^{10} bits or approximately every 6 s. Similarly, when errors occur, block synchronization pulses will be missed, because even with correct block synchronization, one of the "correct" syndromes corresponding to one of the five offset words will not match.

Thus, it is necessary to have some sort of block synchronization flywheel to eliminate spurious synchronization pulses and fill in the missing ones. This could be achieved with any one of the standard strategies, but should take into account the fixed cyclic rhythm of occurrence of the offset words, i.e. A, B, C (or C'), D, A, B, etc.

Bibliography

[1] EBU (1984): *Specifications of the radio data system RDS for VHF/FM sound broadcasting*. Doc. Tech 3244 and Supplements 1 to 4. European Broadcasting Union

[2] WRIGHT, S. *The Broadcaster's Guide to RDS*
Published by Focal Press, Boston, Oxford, Johannesburg, Melbourne, New Delhi, Singapore, 1997, ISBN 0-240-80278-0

[3] KOPITZ, D. and MARKS, B., *RDS – The Radio Data System*
Published by Artech House Publishers, Boston and London, 1999, ISBN 0-89006-744-9

[4] EN 50067, *Specification of the radio data system (RDS for VHF/FM sound broadcasting in the frequency range from 87,5 to 108,0 MHz*

[5] US NRSC-4-B, *National Radio Systems Committee – NRSC-4-A: United States RBDS standard,* 2011

[6] ISO/IEC 7498 (all parts), *Information processing systems – Open Systems Interconnection – Basic Reference Model*

[7] PETERSON, W.W., and BROWN, D.T., *Cyclic codes for error detection*
Proceedings of the IRE, No. 49, January 1961, pp. 228-235

[8] PETERSON, W.W., and WELDON, E.J., *Error-correcting codes*
Published by MIT Press, Cambridge Mass., second edition, 1972

[9] KASAMI, T., *Optimum shortened cyclic codes for burst error correction*
IEEE Transactions on Information Theory (IT9), No. 4, 1963, pp. 105-109

[10] HELLMAN, M.E., *Error detection in the presence of synchronisation loss*
IEEE Transactions on Communications COM-23, No. 5, 1975, pp. 538-539

[11] HELLMAN, M.E., *Error detection made simple*
International Conference on Communication, Minneapolis, Minnesota (USA), June 1974. Conference Record, pp. 9A1-9A4

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